Design and Development of a CPU Scheduler Simulator for Educational Purposes Using SDL

Manuel Rodríguez-Cayetano

Department of Signal Theory and Telematics Engineering
University of Valladolid, ES-47011 Valladolid, Spain
manuel.rodriguez@tel.uva.es

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Summary

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Summary

CPU Scheduling Basics (I)

- CPU scheduling: deciding which of the ready processes is to be allocated the CPU
- Different selection criteria $\Rightarrow$ different scheduling algorithms
- Two types of scheduling algorithms:
  - one queue algorithms: appropriate when all the processes belong to the same class (same scheduling requirements)
  - multilevel queue algorithms: appropriate for processes belonging to several classes (different scheduling requirements)
- Every algorithm may favor one class of process over another due its properties:
  - performance evaluation parameters (throughput, turnaround time, waiting time, ...) are used for comparing CPU scheduling algorithms

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CPU Scheduling Basics (II)

- Selecting an algorithm appropriate for a process workload $\Rightarrow$ evaluation of the algorithms based on values of the performance evaluation parameters
  - for example, select the algorithm that produces the least mean waiting time for a process workload
- Several evaluation methods:
  - deterministic modeling: results only valid for the concrete (deterministic) workload used
  - queuing models based: classes of algorithms and statistical distributions of process parameters limited, results not accurate
  - simulation: can support deterministic and statistical based workloads, results can be more accurate than those obtained using queuing models

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CPU Scheduling Basics (III)

- Simulation consist of programming a model of the computer system that behaves like the actual system (at least regarding CPU scheduling) $\Rightarrow$ modeling:
  - arrival, ready and finished queues
  - clock
  - ...
- Design, coding and debugging of a simulator are usually a major task
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Related work and motivation

- Several CPU scheduling simulators have been previously developed: *CPU Scheduling Simulator*, *CPU Scheduler Application*, *Process Scheduling Simulator*, *MOSS Scheduling Simulator* ...
- Main shortcomings of these simulators:
  - algorithms specific for real-time processes are not supported
  - multilevel queue algorithms are not supported, only single-queue ones
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sdlCPUSched: requirements and assumptions

- Main requirements:
  - simulator for educational purposes, mainly used for behavior and performance analysis of CPU scheduling algorithms
  - support for non real-time and real-time algorithms
  - support for multilevel queue algorithms (number of queues, queue algorithm and queue priority can be configured)
- Main assumptions (to simplify the development of the simulator):
  - all the processes characteristics are independent
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sdlCPUSched: behavior overview

- Signal-based communication between the simulator and its environment
  - interactions are mainly asynchronous (only synchronous during the phase of simulation configuration)
- Input signals:
  - simulation configuration (algorithm simulated, process parameters...)
  - simulation control (start, stop, pause...)
- Output signals:
  - confirmation of simulation configuration
  - notification of simulation events (if verbose mode is selected)
  - values of per-process and global statistics
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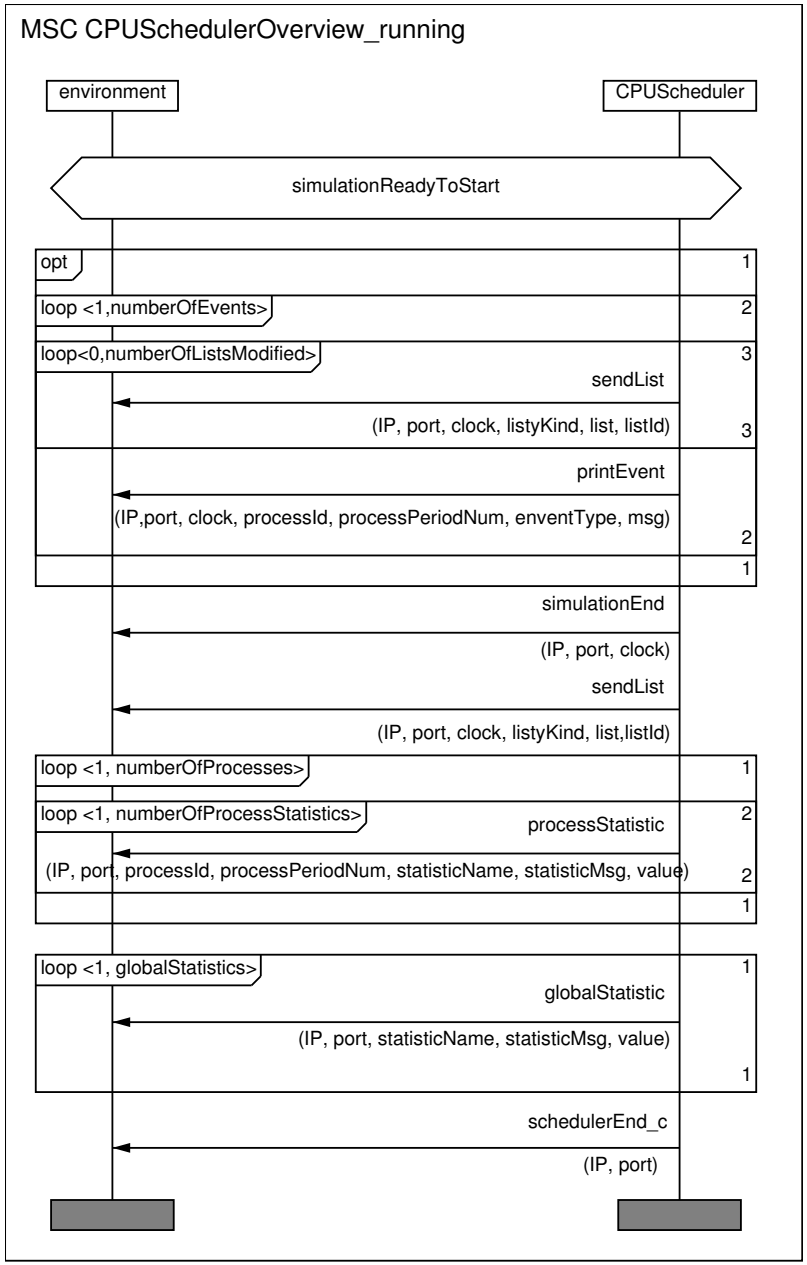
sdlCPUSched: example of an scenario



Simulator structure: motivation issues

- To keep independent intra-queue and inter-queue scheduling functions ⇒ two process types:
  - *MasterSchedulerType* for inter-queue scheduling, one instance
  - *SlaveSchedulerType* for intra-queue scheduling, as many instances as ready queues
- To minimize the amount of code not automatically generated from the SDL specification:
  - one simulator program for all the users using the TCP communication module included in the SDL tool
    - programming communication functions with the system environment is avoided
    - no need to use extra coding in C for sending the port number of every instance of the user's simulator program to its GUI (using files, running program parameters, . . .)
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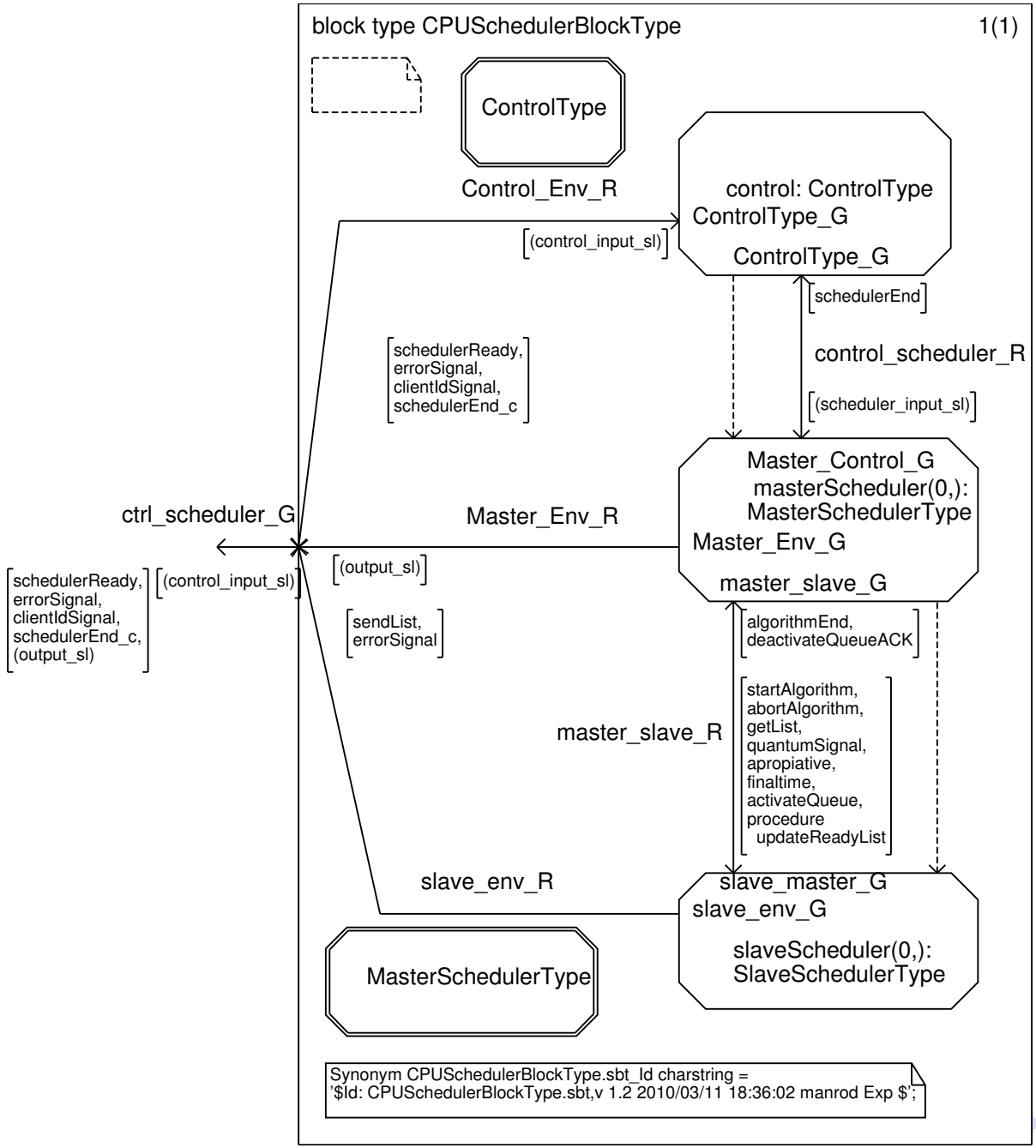
Simulator structure: CPUSchedulerBlockType



Process Type functions

- `controlType` process type:
  - creating a *masterScheduler* process for a simulation requested by one user
  - dispatching signals coming from different users to the corresponding *masterScheduler* process
- `masterSchedulerType`:
  - simulation configuration
  - inter-queues algorithm (the maximum priority non-empty ready queue is activated)
  - access control of the ready queues shared variables
- `slaveSchedulerType`:
  - simulation of a simple (one ready queue) scheduling algorithm
    - finding process arrivals (storing every arrived process in the ready queue)
    - selecting a process from the ready queue to be executed (leaves the ready queue)
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Procedures relating to single-queue algorithms

- Two types of behavior in single queue scheduling algorithms:
  - behavior common to all the algorithms: included in the *genericAlgorithm* procedure
  - algorithm-dependent behavior: included in algorithm specific procedures (one per single-queue algorithm)
- Low level tasks (for example, managing process queues and updating the clock) are specified in auxiliary procedures (*findArrivals*, *executeProcess*, *interruptProcess*, etc.)
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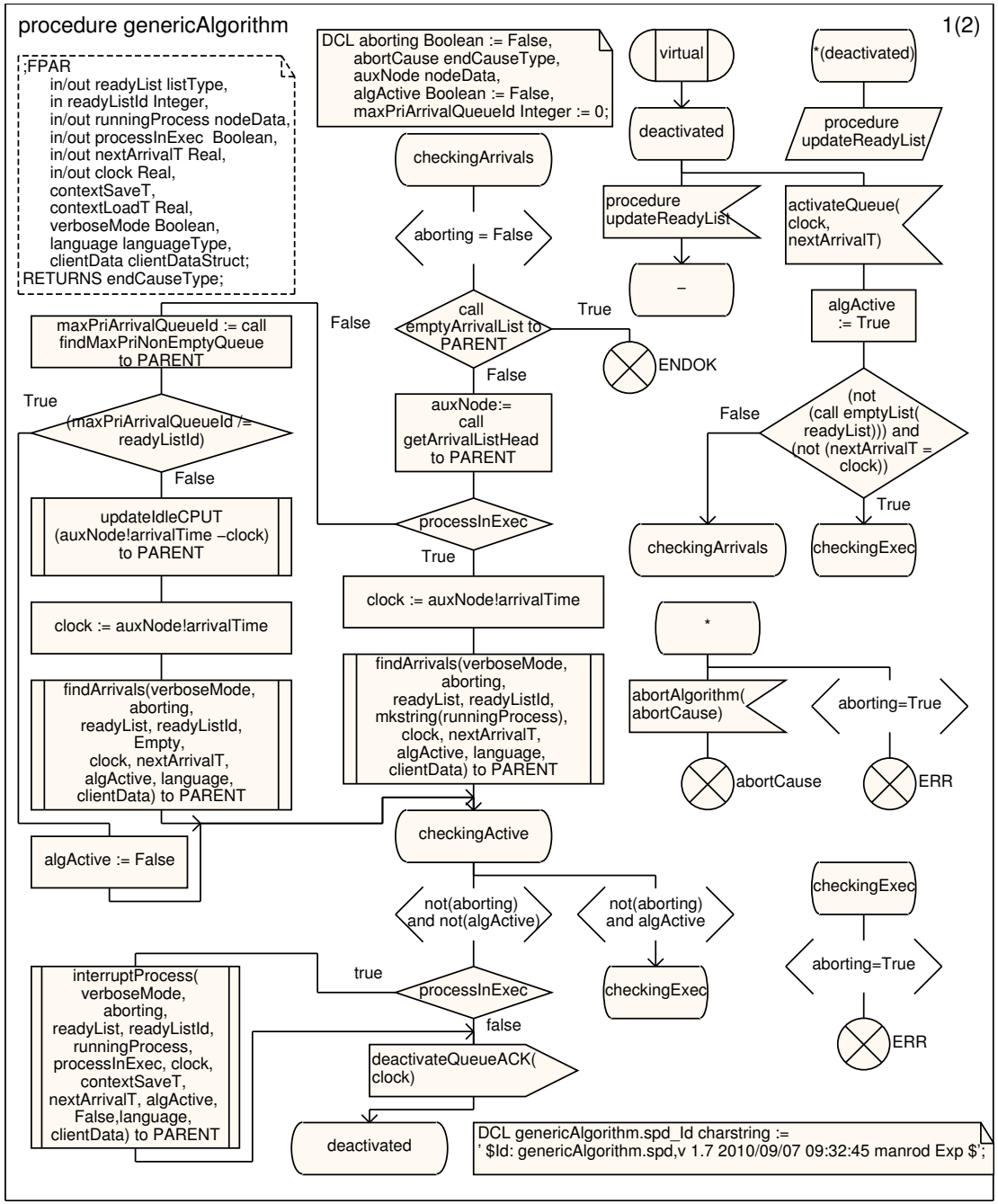
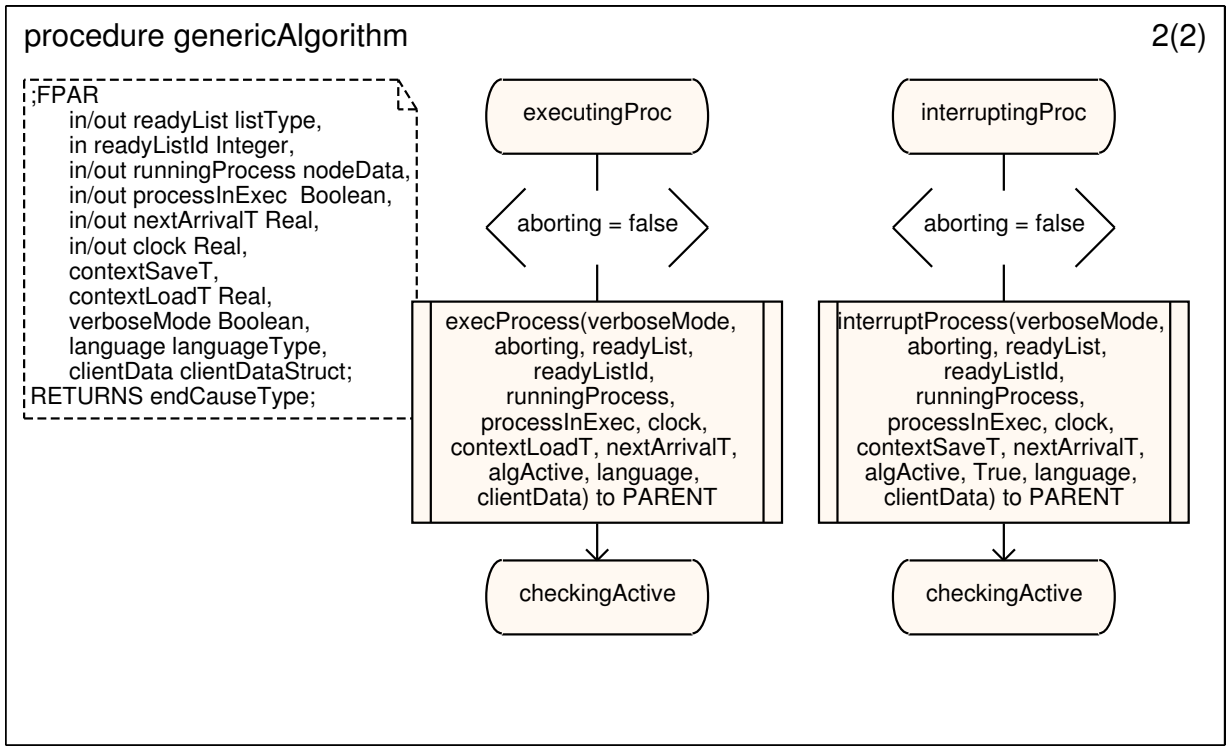
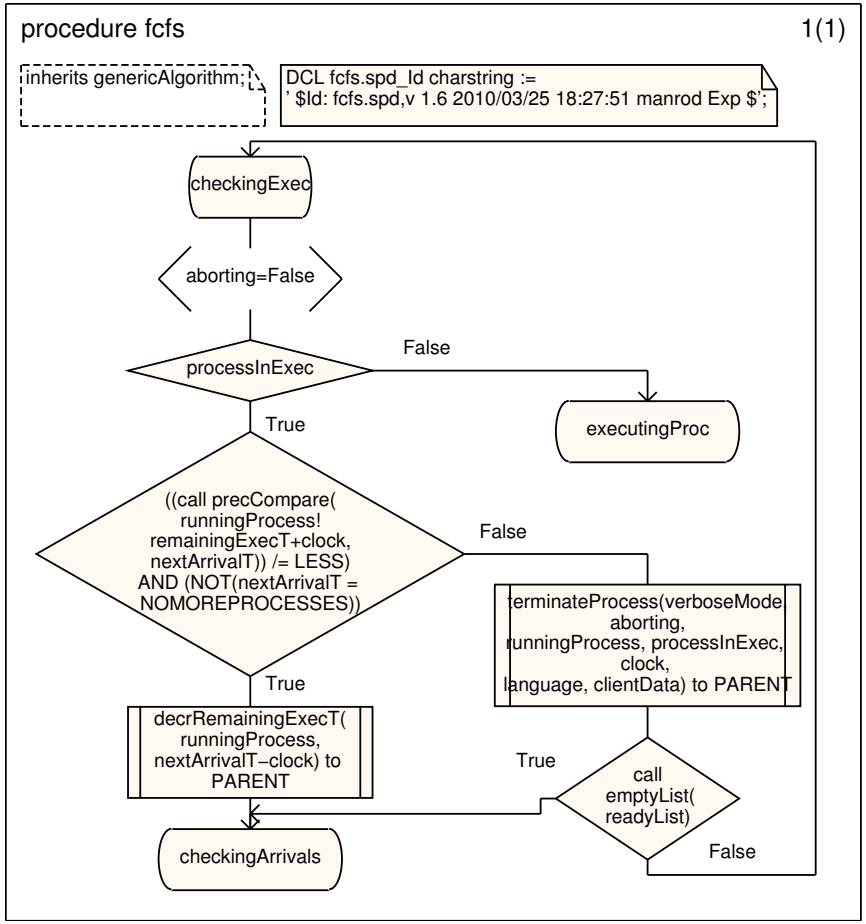


genericAlgorithm procedure specification (II)



An example of an specific algorithm procedure



The CPU Scheduler Simulator Graphical User Interface: *tkCPUSched*

- A graphical user interface (GUI) has been developed to simplify the access to the simulator functionalities
  - simulator program generated from the SDL specification is only accessible through a TCP socket
- GUI developed using Tcl/Tk language
  - interpreted language that provides rapid development of cross-platform graphical user interfaces
- GUI module for parsing simulator outgoing signals:
  - format of the signals interchanged with the environment: Telelogic ASCII encoding (TCP communications module)
    - example: {1}{'schedulerEnd_c'}{{'127.0.0.1',50205}}
  - parsing module based on an automatically generated parser and lexical analyzer
    - parser and lexical analyzer based on a grammar specific to the ASCII encoding: changes in the signal encoding $\Rightarrow$ modifying the grammar and re-generating the parser and lexical analyzer
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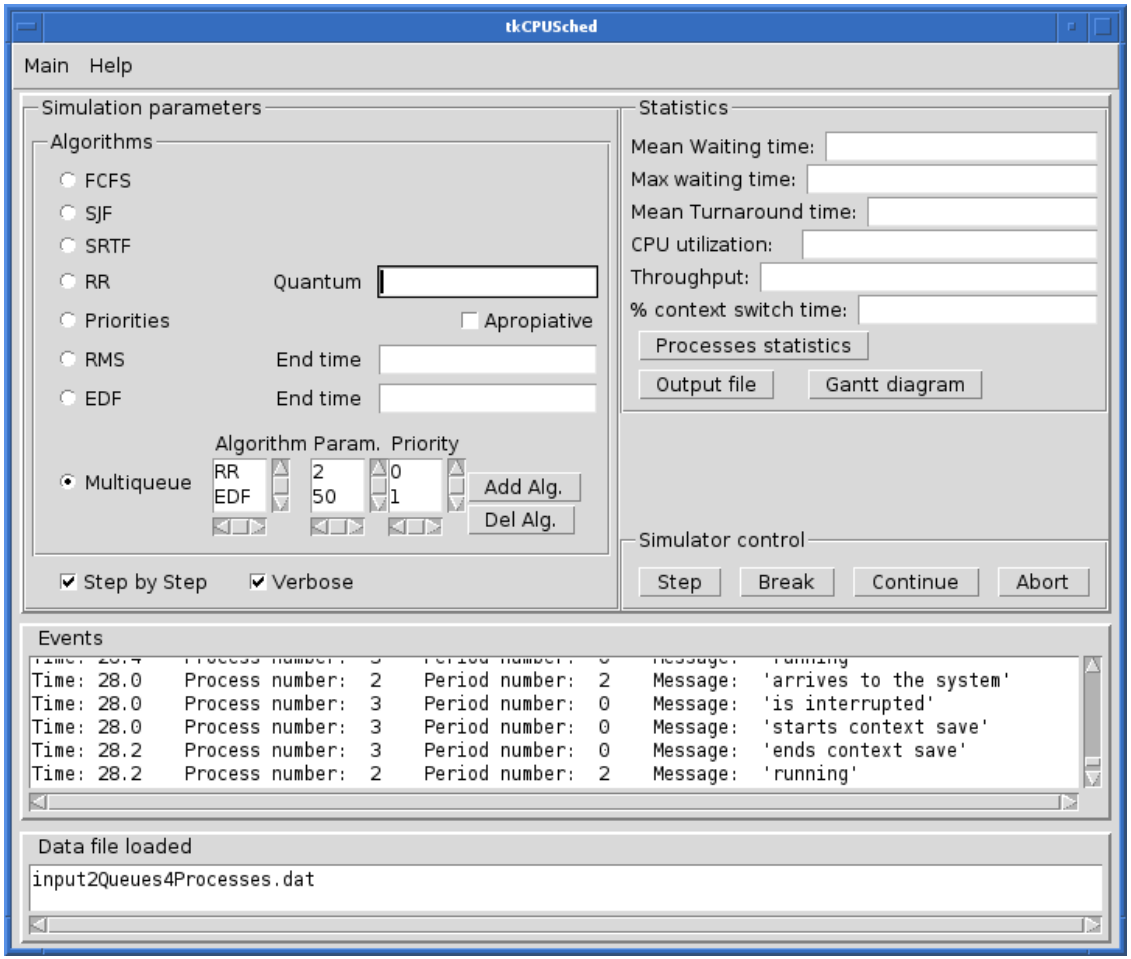

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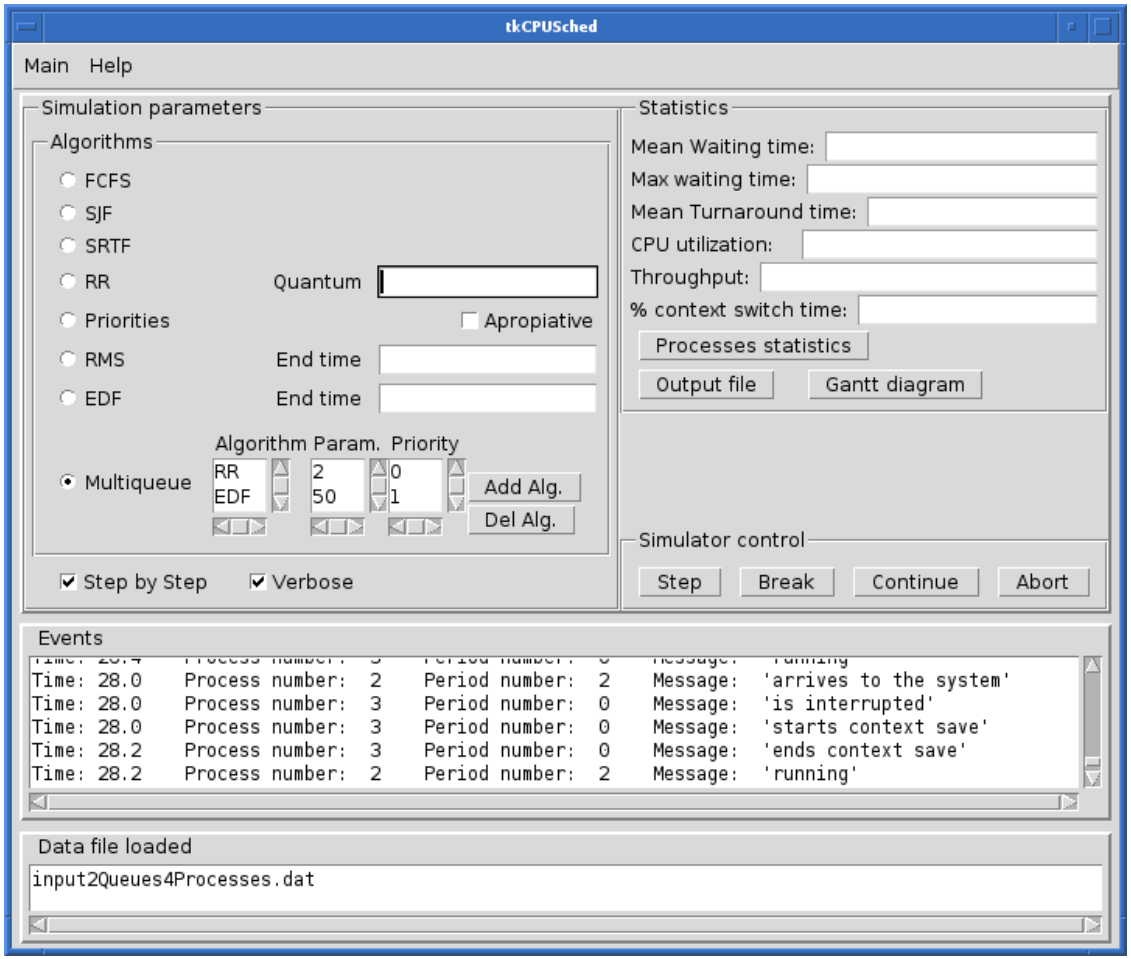

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Questions?